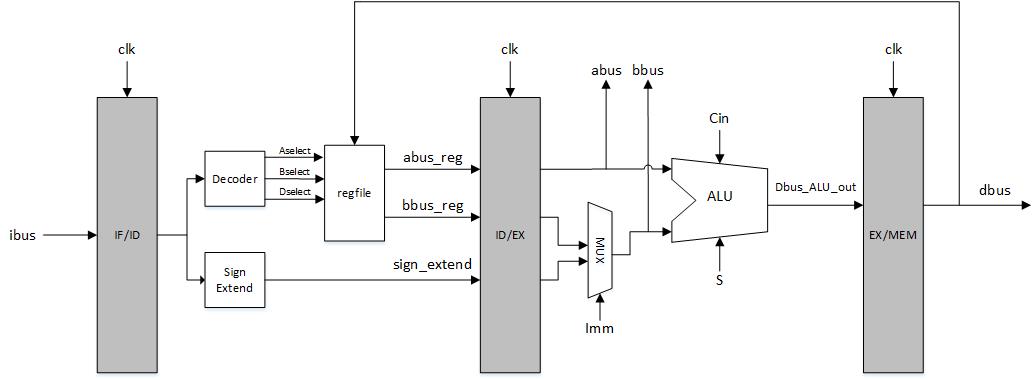
Arjun Gupta

EECE 3324

Lab 5

7/19/2018

1. Description
   1. The main purpose of this lab was to design a 3 stage, 32-bit pipelined CPU. The control signals for this CPU were generated in previous labs and implemented fully in this lab. Sign extended logic was added to represent the sign-extended immediate value as an input to a multiplexor that switched between the register file value and the sign extended value as the second input to the ALU. This multiplexor was also to be added during the execute stage of the pipeline.
2. Block Diagram
   1. The picture below represents the block diagram model for the 3 stage, 32-bit pipelined CPU.
3. Steps taken to complete Assignment
   1. The first step needed to complete this lab was to import the previous labs work into this project. The register file and ALU were needed from lab 3 alongside the controller from lab 4. However, with the structure implemented in the previous labs, the clock cycles were not synced to where they should have been. To solve this, all the signals in between the two D Flip-Flop stages were passed as wires to the top level module, and then passed through a D Flip-Flop from one stage to the other. This allowed the synchronization of all signals going into the pipeline together. This required a significant rewrite of the code structure, but yielded a successful result nonetheless.
4. Lessons learned
   1. This lab took a significant amount of time to complete, since my original code structure was not optimized well for this lab. In order to remedy this, I had to spend a large amount of time debugging using the waveform simulator on Vivado, and learned a lot of skills that will be useful in upcoming labs.

Addendum

Professor Marpaung asked me to upload the picture of this pipeline diagram that I created as a reference for the future. 